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An Explicit Drain Current Model in Subthreshold Regime for Graded Channel Schottky Barrier Gate All Around MOSFET to Improve Analog/RF Performance

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ABSTRACT

In this paper, an explicit analytical model for a Graded Channel Gate All Around Schottky Barrier MOSFET is presented. The problem of carrier mobility degradation in a uniformly highly-doped Schottky Barrier MOSFET is assessed by graded channel architecture in which high doping is considered in the source and low doping in the drain. The Evencent Mode Analysis is carried out using the superposition technique to obtain the surface potential in the channel. The one-dimensional Poisson's and two-dimensional Laplace equations are solved to calculate the surface potential. The subthreshold current is obtained using the surface potential analysis. A TCAD simulator (ATLAS-3D device simulator) is used for numerical simulation purposes. The developed model results are in good agreement with the TCAD simulations.

Keywords: ATLAS-3D, Gaussian graded channel, graded channel, high frequency, surrounding gate MOSFET

INTRODUCTION

In the past decade the Gate All Around MOSFET has received traction as one of the best candidates among existing Multi-Gate MOSFET architecture such as Dual Gate (DG) FET and Fin-FET for ultra-scaled nano devices (Chiang, 2005; Li & Hwang, 2009; Tsormpatzoglou et al., 2009; Zhuge, Wang, Huang, Xing, & Wang, 2008). It offers minimum short channel effects by providing excellent electrostatic control over the entire channel region (Chiang, 2005; Kumar, Haldar, Gupta, & Gupta, 2014a; Kumar, Haldar, Gupta, & Gupta, 2014b). However, the surrounding gate MOSFET reduces SCEs but at the nano-scale the P-N junction depletion width cannot be neglected.

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This junction depletion width is reasonably large and so, resistance at source-channel and drain-channel junctions increases (Kumar, Haldar, Gupta, & Gupta, 2013). To overcome these problems, novel architecture like Schottky Barrier Surrounding Gate MOSFET and Junctionless Surrounding Gate MOSFET are being extensively explored (Colinge et al., 2010; Lee, Zhuang, Di & Han, 2013; Trivedi et al., 2016; Wang, Lou, & Lee, 2013). In Junctionless MOSFET there is no P-N junction and homogeneously doped source-channel-drains are used to avoid junction formation. However, it requires very high metal gate work function to fully deplete a highly-doped channel. Even though the device resolves the problem of junction formation at nanoscale, due to the very high channel doping, Carrier Mobility Degradation (CMD) occurs and degrades device performance compared with when the conventional surrounding gate MOSFET is used (Sharma & Vishvakarma, 2012; Yang et al., 2007).

To overcome all these issues, the Schottky Barrier Surrounding Gate MOSFET has been investigated to discover how improvements can be made (Marchi et al., 2014). The source and drain regions are metallic; this offers reduced source/drain resistance with contact resistivity ($\rho_c \sim 10^{-9}\ \Omega{\cdot}cm$) for metallic S/D compared with $\rho_c \sim 10^{-7}\ \Omega{\cdot}cm$ in doped S/D junction (Pavanello, Martino, Dessard, & Flandre, 2000). The high doping is a problem in the use of the nano-scaled MOSFET due to carrier mobility degradation (CMD). To overcome the problem of CMD, graded channel architecture is proposed and extensively investigated over the conventional surrounding gate MOSFET to improve the performance of the device (Kaur, Kabra, Haldar, & Gupta, 2008; Kumar, Haldar, Gupta, & Gupta, 2016b). In the graded channel architecture, high doping was kept at the source and low doping at the drain.

Recently, Kumar, Haldar, Gupta and Gupta (2016a) proposed a novel Graded Channel Schotttky Barrier GAA MOSFET to reduce carrier mobility degradation. This work extended the development of an analytical model for the calculation of subthreshold current for the GC-SB-GAA MOSFET. In this research work, an analytical model for the Graded Channel Schottky Barrier GAA MOSFET was developed and compared for performance with a conventional uniformly-doped channel with high doping ($N_{A/H} = 5 \times 10^{18}\ cm^{-3}$) Schottky Barrier GAA MOSFET. The device with the Graded Channel (GC) had a high-doping profile in its half-channel region of the source and an undoped channel of the drain. A huge improvement in device performance (in on-state) was observed for the GC-SB-GAA MOSFET structure.

MATERIALS AND METHOD

Simulation and Device Structure

Simulation environment and fabrication feasibility. A schematic view of the Graded Channel (GC) Gate All Around Schottky Barrier (SB) MOSFET is shown in Figure 1. For numerical simulation, the ATLAS 3-D, device simulator (Atlas User's Manual, 2013) was used and the electrical as well as RF characteristics of both devices i.e. SB-GAA MOSFET and GC-SB GAA MOSFET were studied.

The models invoked for the numerical simulation purpose are: SRH recombination/thermal generation model, field dependent mobility (FLDMOB) model for high electric field velocity saturation, concentration dependent mobility (CONMOB) model for concentration dependent

mobility and Boltzmann carrier statistics for electrons and holes. The Newton-Gummel method was adopted for a numerical solution. Cerdeira et al. (2005) have shown the advantages of the graded-channel and the feasibility of fabrication of the proposed device.

Device structure. Figure 1 shows the schematic view of the GC-SB-GAA MOSFET. Two different regions of doping are shown. The following formula was used: Gate length L = 30 nm, radius of Si pillar (R_{Si}) = 10 nm , high Gaussiann doping p-type substrate ($N_{A/H}$) = 5×10^{18} cm^{-3}, low doping p-type substrate ($N_{A/L}$) = 1×10^{15} cm^{-3}, SiO_2 thickness (t_{ox}) = 3 nm, work-function of the metal source/drain $\Phi_{S/D}$ = 4.1 eV, dielectric permittivity of SiO_2 is ε_{ox} = 3.9 and gate metal workfunction Φ_M = 4.8 eV.

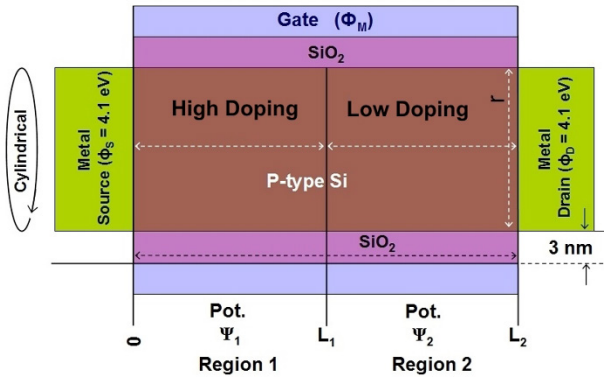


Figure 1. Schematic view of Schottky Barrier Surrounding Gate MOSFET with Gaussian Graded Channel (GGC)

The source side used high doping (5×10^{18} cm^{-3}), while the drain side was left undoped (lightly doped) with silicon (1×10^{15} cm^{-3}). Hence, the potential in these two different regions was also expected to be different. To solve the potential in the two different regions, Poisson's equation was solved for both regions.

Model derivation. The results section was divided into two parts. Part A was analog performance and part B was RF performance of the proposed GGC-SGT-SB-MOSFET.

Surface potential modelling. The silicon under the gate was assumed to be fully depleted. Channel potential including channel mobile carrier density was governed by Poisson's equation in two different regions and is given as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\Phi_j(r,z)\right)+\frac{\partial^2}{\partial z^2}\Phi_j(r,z)=\frac{qN_{AH/AL}}{\varepsilon_{Si}} \quad (1)$$

Here, $\Phi_i(r,z)$ is the potential distribution in the silicon film, q is the electron charge, ε_{Si} is the permittivity of Silicon, i = 1 and 2 shows the undamaged (region-1) and damaged (region-2) regions, respectively. $N_{AH/AL}$ is the doping of silicon film.

Due to the different doping in the two different regions through the channel, the flat band voltage (V_{FBi}) was different in the two different regions (regions 1 and region 2) and were written as:

$$V_{FB1} = \Phi M_1 - \Phi_{Si1};\ i = 1,\ 0 \le z \le L_1 \tag{2}$$

$$V_{FB2} = \Phi M_2 - \Phi_{Si2};\ i = 2,\ L_1 \le z \le (L_1 + L_2) \tag{3}$$

where, Φ_{Si1} and Φ_{Si2} were the semiconductor work function in the two different regions and could be calculated using the generalised equation (Equation 5), and C_{ox} was the gate oxide capacitance per unit area of GME-SB-CGAA MOSFET and was given as:

$$C_{ox} = 2\varepsilon_{ox}\left(t_{Si}\ln\left(1+\frac{2t_{ox}}{t_{Si}}\right)\right)^{-1} \tag{4}$$

and

$$\Phi_{Si} = \chi + (E_g/2) - q\Phi_F \tag{5}$$

where, χ was the electron affinity of the silicon, E_g was the energy band gap and Φ_F was the Fermi potential.

By using the super position technique, the solution of electrostatic potential $\psi_i(r,z)$ could be decomposed in two components, the long channel solution $V_i(r)$ and short channel solution $U_i(r,z)$, where $V_i(r)$ and $U_i(r,z)$ were the solution of the 1D Poisson equation and 2D Laplace equation, respectively. Then, the electrostatic potential in SB-CGAA MOSFET could be written as:

$$\Psi_i(r,z) = V_i(r) + U_i(r,z) \tag{6}$$

Equation 1 was then decomposed to Equations 7 and 8 as:

$$\frac{1}{r}\frac{\partial V_i(r)}{\partial r} + \frac{\partial^2 V_i(r)}{\partial r^2} = \frac{qN_a}{\varepsilon_{si}} \tag{7}$$

$$\frac{1}{r}\frac{\partial U_i(r,z)}{\partial r} + \frac{\partial^2 U_i(r,z)}{\partial r^2} + \frac{\partial^2 U_i(r,z)}{\partial z^2} = 0 \tag{8}$$

where, $i = 1$ for the high-doped region 1 and i = 2 for the low-doped region. The 1D potential $V_i(r)$ could be obtained by solving Poisson's equation with the following boundary conditions:

(a) Potential at the centre of the silicon pillar was:

$$\psi_c\ \Psi_i(r=0,z) = \Psi_c(z) \tag{9a}$$

(b) Electric flux at the centre of the silicon pillar was zero:

$$\frac{\partial}{\partial r}\Psi_i(r=0) = 0 \tag{9b}$$

(c) Potential at the surface of the silicon pillar was:

$$\Psi_i(r,z)\Big|_{r=\frac{t_{Si}}{2}} = \Psi_S(r=\frac{t_{Si}}{2},z) \tag{9c}$$

(d) Electric flux at the surface of the silicon pillar was continuous:

$$\frac{\partial}{\partial r}\Psi_i(r,z)\Big|_{r=\frac{t_{Si}}{2}} = \frac{C_{ox}}{\varepsilon_{Si}}\left[V_{GS} - V_{FBi} - \Psi_i(r=\frac{t_{Si}}{2},z)\right] \tag{9d}$$

The solution of the 1D Poisson equation (Equation 7) using the boundary conditions given in Equations 9a-9d can be expressed as:

$$V_1(r) = \frac{qN_{A/H}}{4\varepsilon_{Si}}r^2 + V_{GS} - [\phi_M - \phi_{Si1}] - \frac{qN_{A/H}t_{Si}^2}{16\varepsilon_{Si}} - \frac{qN_{A/H}t_{Si}}{4\beta\varepsilon_{Si}} \tag{10a}$$

and

$$V_2(r) = \frac{qN_{A/L}}{4\varepsilon_{Si}}r^2 + V_{GS} - [\phi_M - \phi_{Si2}] - \frac{qN_{A/L}t_{Si}^2}{16\varepsilon_{Si}} - \frac{qN_{A/L}t_{Si}}{4\beta\varepsilon_{Si}} \tag{10b}$$

Here, V_{GS} was the gate-to-source voltage; t_{si} was the diameter of the silicon pillar and $\beta=C_{ox}/\varepsilon_{Si}$. The solution of the 2D Laplace equation (Equation 8) was obtained using the following boundary conditions:

(a) At the interface of two different metal gates, potential is continuous.

$$\Psi_1(r,z)\Big|_{z=L_0} = \Psi_2(r,z)\Big|_{z=L_0} \tag{11a}$$

(b) At the interface of M_1 and M_2, the electric field is continuous.

$$\frac{\partial}{\partial r}\Psi_1(r,z)\Big|_{z=L_0} = \frac{\partial}{\partial r}\Psi_2(r,z)\Big|_{z=L_0} \tag{11b}$$

(a) Potential at the source end could be taken as:

$$\Psi_i(r,z=0) = V_{bi,S/D} - \Delta\Phi_{bS} \tag{11c}$$

(c) Potential at the drain end could be taken as:

$$\Psi_i(r,z=L_0+L_1) = V_{bi,S/D} - \Delta\Phi_{bD} + V_{DS} \tag{11d}$$

Here, $V_{bi,S/D}$ was the built-in potential at source/drain and $\Delta\Phi_{bS}$ and $\Delta\Phi_{bD}$ were SB lowering at source and drain, respectively (Crowell & Rideout, 1969; Kumar et al., 2016b). It could be expressed as:

$$V_{bi,S/D} = \Phi_{Si} - \Phi_{S/D} \tag{12}$$

$$\Delta\Phi_{bS} = \alpha\left[\frac{\tau q}{4\pi\varepsilon_S}\right]^{\frac{1}{2}} E_S^{\frac{1}{2}} \tag{13a}$$

$$\Delta\Phi_{bD} = \alpha\left[\frac{\tau q}{4\pi\varepsilon_S}\right]^{\frac{1}{2}} E_D^{\frac{1}{2}} \tag{13b}$$

Here, χ was the electron affinity of silicon, ε_{Si} was the silicon permittivity and E_S and E_D were the electric field at the source and drain end, respectively. α and τ were treated as a fitting parameter (α =1, τ = 1.1).
The solution of Equation 8 using the above boundary conditions can be expressed as:

$$U_i(r,z) = \sum_{n=1}^{\infty} J_0(\lambda_n r)\left(\mathrm{A}_i e^{\lambda_n z} + \mathrm{B}_i e^{-\lambda_n z}\right) \tag{14}$$

A_1, A_2, B_1 and B_2 are the Bessel-Fourier series coefficients and are given in the Appendix. Υ_n is the Eigen value satisfying the following equation:

$$C_{ox} J_0\left(\Upsilon_n \frac{t_{Si}}{2}\right) - \varepsilon_{si} \Upsilon_n J_1\left(\Upsilon_n \frac{t_{Si}}{2}\right) = 0 \tag{15}$$

J_0 and J_1 are the Bessel function of order zero and one, respectively.

Subthreshold current modelling. The total subthreshold current was due to the thermionic current and the tunneling currents and are given as:

$$I_{Thermionic} = \pi t_{Si} \mu k T n_i \frac{(1 - e^{\left(\frac{-V_{DS} q}{kT}\right)})}{\left[\int_0^L \left[\frac{1}{\int_0^R e\left[\frac{(\Psi(r, V_{DS}, V_{GS}, z))}{kT}\right] dr}\right] dz\right]} \tag{16}$$

and

$$I_{Tunneling} = \pi t_{Si} A^* T^2 e^{\left(\frac{-\phi_b}{E_{00}(\phi_b)}\right)} (e^{\left(\frac{V_{gs} q}{nkT}\right)} - 1) \tag{17}$$

Here, μ (1300 cm^2/Vs) was the mobility, n_i (1.45×10^{10} cm^{-3}) was the intrinsic carrier concentration, A^* was the Richardson constant, ϕ_b was the barrier height, and E_{00} was the constant of the material associated with the WKB expression and was given as (Balaguer, Iniguez, & Roldan, 2011):

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{18}$$

$$E_{00} = \alpha(\Phi_b) q \frac{\hbar}{2} \sqrt{\frac{N_A}{m^* \varepsilon_{Si}}} \tag{19}$$

$$\alpha(\Phi_b) = G + H\Phi_b \tag{20a}$$

$$\hbar = h / 2\pi \tag{20b}$$

Here, m^* was the effective mass of the electron, k was the Boltzmann constant and h was the Plank constant. G and H were the fitting parameters, with the values 21.8 (1/ eV) and 36.6 (1/ eV) (Balaguer et al., 2011).

The total subthreshold current was the combination of both $I_{thermionic}$ and $I_{tunneling}$ (Balaguer et al., 2011) and was evaluated as:

$$I_{Sub_total} = \frac{(I_{thermionic} I_{Tunneling})}{(I_{thermionic} + I_{Tunneling})} \tag{21}$$

RF performance. Cut-off frequency (fT) was the important parameter for evaluating the RF performance of the device and it was a good candidate for high-frequency switching applications.

RESULTS

The surface potential of any device is a characteristic by which we can calculate the threshold voltage of the device. The surface potential at no applied bias is shown in Figure 2. It can be observed that the surface potential for the proposed SB-GC MOSFET device shifts upwards and the minimum of the surface potential lies under the highly-doped region of the MOSFET. The upward shift of the surface potential indicated that the threshold voltage of the graded channel device would be lower compared to that of the uniformly-doped device. The analytical result presented in the figure for the proposed device was in good agreement with the simulation results obtained through the ATLAS-3D numerical simulation tool. The surface potential was also calculated for applied bias and it was observed that the minimum surface potential still lay in the highly-doped region. The analytical and simulation results were matched.

DISCUSSION

The electric field for both the devices is shown in Figures 4(a) and 4(b) at no bias applied and at applied bias, respectively. From Figure 4(a) and 4(b) it is evident that the electric field towards the drain end was lowered for the Graded Channel Schottky Barrier GAA MOSFET. This means that the reduced electric field resulted in reduced short channel effects. This was the result of lower carrier mobility degradation.

The subthreshold drain current for the Graded Channel Schottky Barrier Gate All Around MOSFET is shown in Figure 5. The analytical model results were in good agreement with the simulation results. The figure also depicts that the on current of the graded channel was drastically increased by 47%; this is desirable in scaled MOSFET devices. Due to the lower doping towards the drain side, carrier mobility was enhanced compared with that of the uniformly-doped channel SB-MOSFET. Consequently, the on-state current increased. This was also mainly due to the reduced resistance in the undoped part of the channel region.

However, one tradeoff observed in the Graded Channel SB-GAA MOSFET was that the off-state current was increased, reducing the I_{on}/I_{off} ratio of the device. This indicated that the device would be better used in analog applications and would degrade performance compared to SB-GAA MOSFET for digital applications. In the triode region of operation, the Graded Channel MOSFET had higher current than the conventional MOSFET. This was due to the slightly higher surface electron concentration as well as to higher mobility in the low-doped region. In addition, current density was concentrated near the surface of the high-doped part of the channel but spread inside the low-doped region, contributing to reducing the resistance associated with the low-doped region of the MOSFET.

The high on-current resulted in higher transconductance; thus, the high cut-off frequency for the Graded Channel SB-GAA MOSFET was expected. Figure 6 shows the simulated transconductance for both the devices and it clearly depicts that the graded channel device consisted of high transconductance. It is clear from the figure that the GC-SB-GAA MOSFET showed higher transconductance than the SB-GAA MOSFET. The improvement in transconductance was directly related to the improvement in the low-frequency open-loop gain of the device and can be expressed as $A_V=(g_m/I_{DS})V_{EA}$. The enhanced transconductance of the GC-SB-GAA MOSFET can provide very high gain and can be used in operational amplifiers. Figure 7 illustrates the variation of cut-off frequency with gate voltage for both the devices and it was clearly observed that the peak cut-off frequency of the GC-SB-GAA architecture was 260 GHz, while for SB-GAA, it was 196 GHz, respectively. This clearly shows that the graded channel architecture improved the peak cut-off frequency by 32%. It was expected that the increased transconductance would increase the cut-off frequncy, as can be seen in Figure 7.

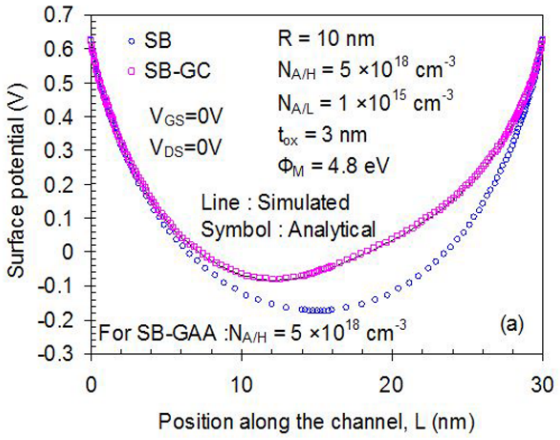


Figure 2. Variation of surface potential for both SB-GAA and GC-SB-GAA MOSFET at no applied bias

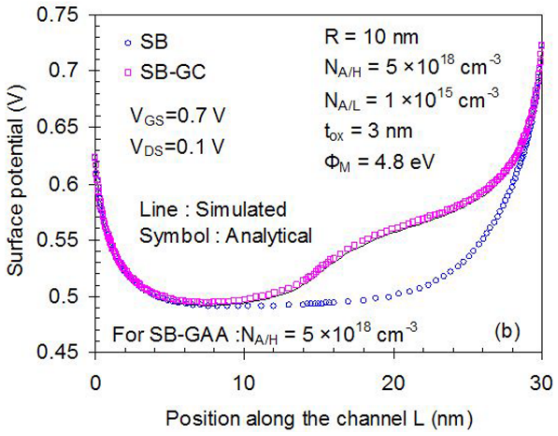


Figure 3. Variation of surface potential for both SB-GAA and GC-SB-GAA MOSFET at V_{GS} = 0.7V and V_{DS} = 0.1V

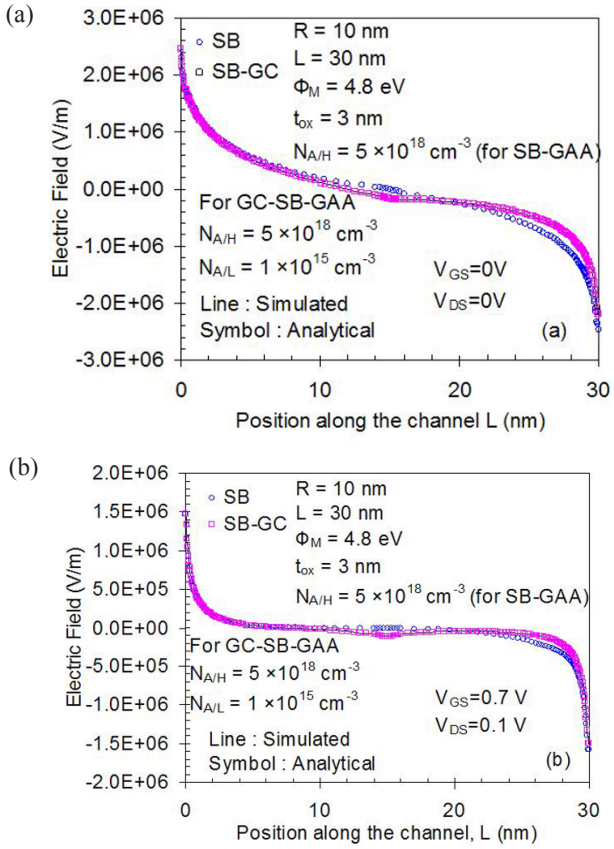


Figure 4. Variation of electric field: (a) at no applied bias; (b) at V_{GS} = 0.7V and; V_{DS} = 0.1V for SB-GAA and GC-SB-GAA MOSFET

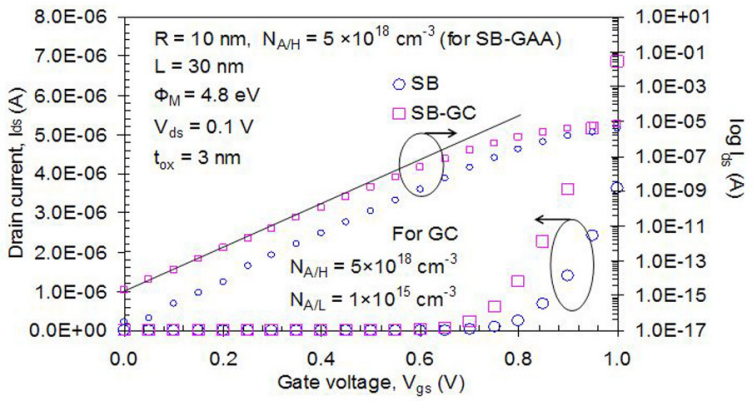


Figure 5. Variation of drain current (I_{ds}) at normal scale versus gate voltage V_{GS} at a fixed drain bias of 0.1 V

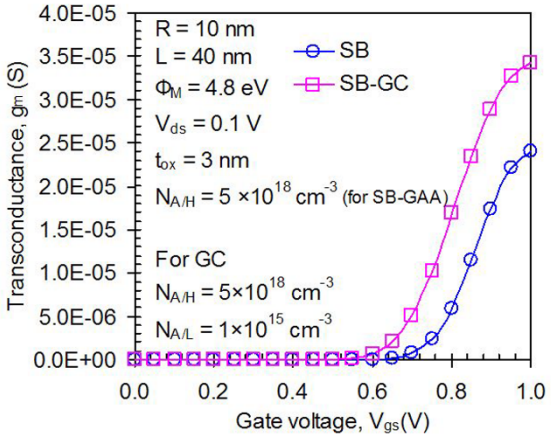


Figure 6. Variation of transconductance with applied gate voltage (V_{gs}) at a fixed V_{DS} of 0.1 V

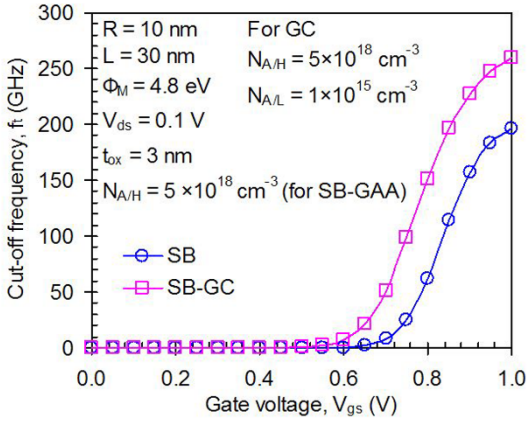


Figure 7. Variation of cut-off frequency as a function of the applied gate bias V_{gs}

CONCLUSION

The Graded Channel (GC) Schottky Barrier Gate All Around MOSFET offered better on-state performance compared to the conventional highly-doped Schottky Barrier Gate All Around MOSFET in terms of I_{on}, g_m and high cut-off frequency. The on-current was improved by 47%, resulting in higher transconductance. The cut-off frequency of the device was improved by 32%. The developed analytical model using the superposition technique showed good agreement with the ATLAS-3D simulation results. So, it was concluded that the Graded Channel (GC) Schottky Barrier Gate All Around MOSFET was a strong contender for low-power high performance devices applicable in future USLI (Ultra Large Scale Integration) applications.

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REFERENCES

ATLAS User's Manual. (2013). *3D Device Simulator, Silvaco Inc., Santa Clara, CA, USA*. Retrieved from the Silvaco website: https://www.silvaco.com/products/vwf/atlas/device3d/device3d_br.html

Balaguer, M., Iniguez, B., & Roldan, J. B. (2011). An analytical compact model for Schottky-barrier double gate MOSFETs. *Solid State Electronics, 64*(1), 78–84. https://doi.org/10.1016/j.sse.2011.06.045

Cerdeira, A., Aleman, M. A., Pavanello, M. A., Martino, J. A., Vancaillie, L., & Flandre, D. (2005). Advantages of the graded-channel SOI FD MOSFET for application as a quasi-linear resistor. *IEEE Transactions on Electron Devices*, *52*(5), 967–972. doi: 10.1109/TED.2005.846327

Chiang, T. K. (2005). A compact analytical two-dimensional threshold voltage model for cylindrical, fully depleted, surrounding-gate (SG) MOSFETs. *Semiconductor Science and Technology, 20*(12), 1173–1178. doi: 10.1109/EDSSC.2005.1635330

Colinge, J. P., Lee, C. W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., … & Murphy, R. (2010). Nanowire transistors without junctions. *Nature Nanotechnology, 5*(3), 225–229. doi: 10.1038/nnano.2010.15

Crowell, C. R., & Rideout, V. L. (1969). Normalized thermionic-field (TF) emission in metal-semiconductor (Schottky) barriers. *Solid-State Electronics, 12*(2), 89–105. https://doi.org/10.1016/0038-1101(69)90117-8

Kaur, H., Kabra, S., Haldar, S., & Gupta, R. S. (2008). An analytical threshold voltage model for graded channel asymmetric gate stack (GCASYMGAS) surrounding gate MOSFET. *Solid State Electronics, 52*(2), 305–311. doi: 10.1016/j.sse.2007.09.006

Kumar, M., Haldar, S., Gupta, M., & Gupta, R. S. (2013). A comparative assessment of Schottky-barrier source/drain GAA MOSFET with conventional and junctionless GAA MOSFETs. *IEEE Indian Conference (INDICON)* (pp. 1–6). Indian Institute of Technology, Bombay: India. doi: 10.1109/INDCON.2013.6726127

Kumar, M., Haldar, S., Gupta, M., & Gupta, R. S. (2014a). Impact of gate material engineering (GME) on analog/rf performance of nanowire Schottky-barrier gate all around (GAA) MOSFET for low power wireless applications: 3D T-CAD simulation. *Microelectronics Journal, 45*(11)*,* 1508–1514. doi: 10.1016/j.mejo.2014.07.010

Kumar, M., Haldar, S., Gupta, M., & Gupta, R. S. (2014b). A new t-shaped source/drain extension (T-SSDE) gate underlap GAA MOSFET with enhanced subthreshold analog/rf performance for low Power applications. *Solid State Electronics Journal, 101,* 13–17.

doi: 10.1016/j.mejo.2014.07.010

Kumar, M., Haldar, S., Gupta, M., & Gupta, R. S. (2016a, November 4–5). Gaussian graded channel (GGC) Schottky-barrier surrounding gate MOSFET for analog/rf performance enhancement. *ICANN 2016*. Retrieved from http://www.icannjmi.in/index.php

Kumar, M., Haldar, S., Gupta, M., & Gupta, R. S. (2016b). Physics-based analytical model for surface potential and subthreshold current of cylindrical Schottky-barrier gate all around MOSFET with high-k gate stack. *Superlattices and Microstructures, 90,* 215–226. doi: 10.1016/j.spmi.2015.12.029

Lee, C., Zhuang, Y., Di, S., & Han, R. (2013). Subthreshold behavior models for nanoscale short-channel junctionless cylindrical surrounding-gate MOSFETs. *IEEE Electron Device Letters, 60*(11), 3655–3662. doi: 10.1109/TED.2013.2281395

Li, Y., & Hwang, C. H. (2009). The effect of the geometry aspect ratio on the silicon ellipse-shaped surrounding – Gate field-effect transistor and circuit. *Semiconductor Science and Technology, 24*(9), 095018. doi:10.1088/0268-1242/24/9/095018.53

Marchi, M. D., Sacchetto, V., Zhang, J., Frache, S., Gaillardon, P. E., Leblebici, Y., & Micheli, G. D. (2014). Top-Down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity. *IEEE Transactions on Nanotechnology, 13*(6), 1029–1038. doi: 10.1109/TNANO.2014.2363386

Pavanello, M. A., Martino, J. A., Dessard, V., & Flandre, D. (2000). Analog performance and application of graded-channel fully depleted SOI MOSFETs. *Solid State Electronics, 44*(7)*,* 1219–1222. doi: 10.1016/S0038-1101(00)00034-4

Sharma, D., & Vishvakarma, S. K. (2012). Precise analytical model for short channel cylindrical gate (CylG) vgate-al-around (GAA) MOSFET. *Solid State Electronics, 86,* 68–74. doi: org/10.1016/j.sse.2012.08.006

Trivedi, N., Kumar, M., Haldar, S., Deswal, S. S., Gupta, M., & Gupta, R. S. (2016). Analytical modeling of junctionless accumulaion mode cylindrical surrounding gate MOSFET. *International Journal of Numerical Modeling Electronic Networks Devices and Fields, 29*(6), 1036–1043. doi: 10.1002/jnm.2162

Tsormpatzoglou, A., Tassis, D. H., Dimitriadis, C. A., Ghibaudo, G., Pananakakis, G., & Clerc, R. (2009). A compact drain current model of short-channel cylindrical gate-all-around MOSFETs. *Semiconductor Science and Technology, 24*(7)*,* 075017. doi: 10.1088/0268-1242/24/7/075017

Wang, T., Lou, L., & Lee, C. (2013) A junctionless gate-all-around silicon nanowire FET of high linearity and its potential applications. *IEEE Electron Devices Letter, 34*(4), 478–480. doi: 10.1109/LED.2013.2244056

Yang, W., Whang, S., Lee, S., Zhu, H., Gu, H., & Cho, B. (2007). Schottky-Barrier Si nanowire MOSFET: Effects of source/drain metals and gate dielectrics. *Materials Research Society Symposium Proceedings* (pp. 133–138). doi: 10.1557/PROC-1017-DD14-05

Zhuge, J., Wang, R., Huang, R., Xing, Z., & Wang, Y. B. (2008). Investigation of parasitic effects and design optimization in silicon nanowire MOSFETs for rf applications. *IEEE Transactions on Electron Devices*, *55*(8), 2142–2147. doi: 10.1109/TED.2008.926279

APPENDIX

The coefficients of Equations 10-15 are:

$$m = \frac{t_{Si}}{2}\ , \kappa = V_{GS} - \frac{qN_A t_{Si}^2}{16\varepsilon_{Si}} - \frac{qN_A t_{Si}}{4\varepsilon_{Si}\beta},$$

$$X = \frac{qt_{Si}^2}{16\varepsilon_{Si}}(N_{A/H} - N_{A/L}) + \frac{qt_{Si}}{4\varepsilon_{Si}\beta}(N_{A/H} - N_{A/L}) + \Phi_{Si1} - \Phi_{Si2} + \frac{qr^2}{4\varepsilon_{Si}}(N_{A/L} - N_{A/H})$$

$$P = \frac{V_{biS} m J_1(\lambda_{n1} m)}{\lambda_n} - \frac{m J_1(\lambda_n m)}{\lambda_n}\left\{V_{GS} - (\Phi_M - \Phi_{Si1}) - \frac{qN_{A/H} t_{Si}^2}{16\varepsilon_{Si}} - \frac{qN_{A/H} t_{Si}}{4\varepsilon_{Si}\beta} + \frac{qN_{A/H} m^2}{4\varepsilon_{Si}}\right\} + \frac{qN_{A/H} m^2 J_2(\lambda_n m)}{2\varepsilon_{Si}\lambda_n^2}$$

$$Q = \frac{(V_{biS} + V_{DS}) m J_1(\lambda_n m)}{\lambda_n} - \frac{m J_1(\lambda_n m)}{\lambda_n}\left\{V_{GS} - (\Phi_M - \Phi_{Si2}) - \frac{qN_{A/L} t_{Si}^2}{16\varepsilon_{Si}} - \frac{qN_{A/L} t_{Si}}{4\varepsilon_{Si}\beta} + \frac{qN_{A/L} m^2}{4\varepsilon_{Si}}\right\} + \frac{qN_{A/L} m^2 J_2(\lambda_n m)}{2\varepsilon_{Si}\lambda_n^2}$$

$$B_2 = -\sinh^{-1}(\lambda(L_1 + L_2))\left[\frac{2}{m^2 J_1^2(\lambda m)}[Q - Pe^{\lambda(L_1+L_2)}] + \frac{2X\cosh(\lambda L_1)e^{\lambda(L_1+L_2)}}{\lambda m J_1(\lambda m)}\right]$$

$$B_1 = \frac{X}{e^{-\lambda L_1} m\lambda J_1(\lambda m)} - \sinh^{-1}(\lambda(L_1 + L_2))\left[\frac{2}{m^2 J_1^2(\lambda m)}[Q - Pe^{\lambda(L_1+L_2)}] + \frac{2X\cosh(\lambda L_1)e^{\lambda(L_1+L_2)}}{\lambda m J_1(\lambda m)}\right]$$

$$A_1 = \frac{2P}{m^2 J_1^2(\lambda m)} - \frac{X}{e^{-\lambda L_1} m\lambda J_1(\lambda m)} + \sinh^{-1}(\lambda(L_1 + L_2))\left[\frac{2}{m^2 J_1^2(\lambda m)}[Q - Pe^{\lambda(L_1+L_2)}] + \frac{2X\cosh(\lambda L_1)e^{\lambda(L_1+L_2)}}{\lambda m J_1(\lambda m)}\right]$$

$$A_2 = A_1 - \frac{X}{e^{\lambda L_1} m\lambda J_1(\lambda m)}$$